PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H04B 7/08

A1

(11) International Publication Number: WO 98/32243

(43) International Publication Date: 23 July 1998 (23.07.98)

(21) International Application Number: PCT/US97/22042

(22) International Filing Date: 8 December 1997 (08.12.97)

(30) Priority Data:
08/773,560 27 December 1996 (27.12.96) US

(71) Applicant: ERICSSON INC. [US/US]; 7001 Development Drive, P.O. Box 13969, Research Triangle Park, NC 27709 (US).

(72) Inventors: BOTTOMLEY, Gregory, Edward; 100 Merlot Court, Cary, NC 27511 (US). CHENNAKESHU, Sandeep; 311 Glen Abbey Drive, Cary, NC 27513 (US).

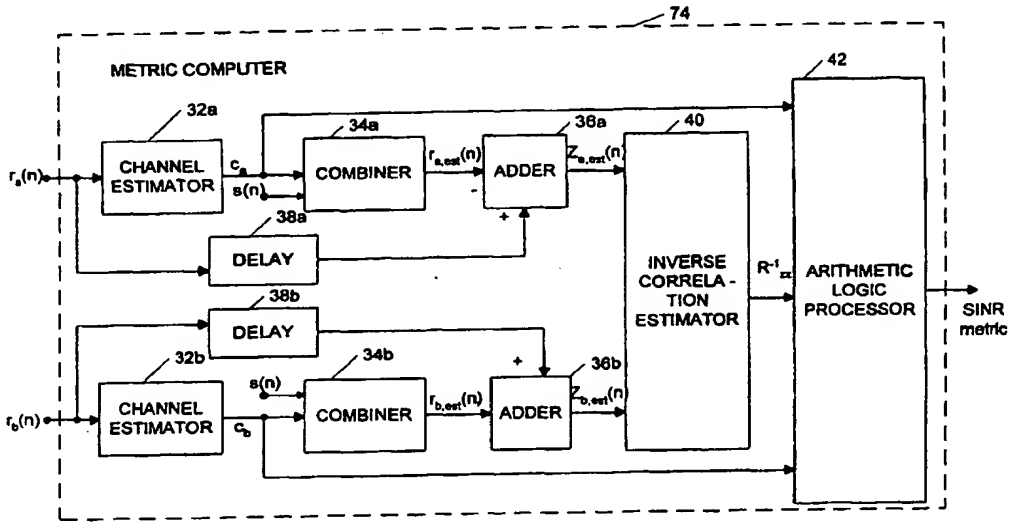
(74) Agents: HALL, David, C. et al.; Ericsson Inc., 7001 Development Drive, P.O. Box 13969, Research Triangle Park, NC 27709 (US).

(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZW, ARIPO patent (GH, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).

Published
With international search report.

(54) Title: METHOD AND APPARATUS FOR JOINT SYNCHRONIZATION OF MULTIPLE RECEIVE CHANNELS

(57) Abstract



An apparatus for joint synchronization of digital communication signals from multiple receive channels is disclosed. In one embodiment, the apparatus comprises a control unit, a metric computer, a decimator and a switch. The control unit generates test sampling phase vectors for use in decimating the signals. The output of the decimator is used by the metric computer to form a metric predictive of the performance of a demodulator. The metric is used by the control unit to select an optimal sampling phase vector. In one embodiment, the metric computer calculates the signal to impairment plus noise ratio (SINR) at the output of the demodulator based on the decimated signals. An inverse correlation estimator may be used to generate an inverse impairment correlation estimate for use in calculating output SINR. In one embodiment, a data correlation estimator generates a data correlation estimate for use in calculating output SINR. The switch controls the communication of decimated signals to the interference canceling processor. In another embodiment, the apparatus includes a select unit and a metric computer. The select unit may include a control unit and a decimator. The metric computer also includes at least one decimator. Test sampling phase vectors are provided to the metric computer along with the input signals. The metric computer generates a metric predictive of the performance of the interference canceling processor and passes the metric to the control unit. The control unit selects a test sampling phase vector that optimizes performance of the interference canceling processor and passes the selected vector to the decimator, which decimates the input signals according to the sampling phases of the selected sampling phase vector. A method of joint synchronization of signals from multiple receive channels is also disclosed.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT

AL	Albania	**ES**	Spain	**LS**	Lesotho	**SI**	Slovenia
AM	Armenia	**FI**	Finland	**LT**	Lithuania	**SK**	Slovakia
AT	Austria	**FR**	France	**LU**	Luxembourg	**SN**	Senegal
AU	Australia	**GA**	Gabon	**LV**	Latvia	**SZ**	Swaziland
AZ	Azerbaijan	**GB**	United Kingdom	**MC**	Monaco	**TD**	Chad
BA	Bosnia and Herzegovina	**GE**	Georgia	**MD**	Republic of Moldova	**TG**	Togo
BB	Barbados	**GH**	Ghana	**MG**	Madagascar	**TJ**	Tajikistan
BE	Belgium	**GN**	Guinea	**MK**	The former Yugoslav Republic of Macedonia	**TM**	Turkmenistan
BF	Burkina Faso	**GR**	Greece			**TR**	Turkey
BG	Bulgaria	**HU**	Hungary	**ML**	Mali	**TT**	Trinidad and Tobago
BJ	Benin	**IE**	Ireland	**MN**	Mongolia	**UA**	Ukraine
BR	Brazil	**IL**	Israel	**MR**	Mauritania	**UG**	Uganda
BY	Belarus	**IS**	Iceland	**MW**	Malawi	**US**	United States of America
CA	Canada	**IT**	Italy	**MX**	Mexico	**UZ**	Uzbekistan
CF	Central African Republic	**JP**	Japan	**NE**	Niger	**VN**	Viet Nam
CG	Congo	**KE**	Kenya	**NL**	Netherlands	**YU**	Yugoslavia
CH	Switzerland	**KG**	Kyrgyzstan	**NO**	Norway	**ZW**	Zimbabwe
CI	Côte d'Ivoire	**KP**	Democratic People's Republic of Korea	**NZ**	New Zealand		
CM	Cameroon			**PL**	Poland		
CN	China	**KR**	Republic of Korea	**PT**	Portugal		
CU	Cuba	**KZ**	Kazakstan	**RO**	Romania		
CZ	Czech Republic	**LC**	Saint Lucia	**RU**	Russian Federation		
DE	Germany	**LI**	Liechtenstein	**SD**	Sudan		
DK	Denmark	**LK**	Sri Lanka	**SE**	Sweden		
EE	Estonia	**LR**	Liberia	**SG**	Singapore		

METHOD AND APPARATUS FOR JOINT SYNCHRONIZATION OF MULTIPLE RECEIVE CHANNELS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to the communication of digital signals and more specifically to receiver synchronization of multiple diversity channels in a digital communication system.

2. Description of Related Art

In digital communication systems, digital symbols, such as binary ±1 values, are transmitted as waveforms through a channel from a transmitter to a receiver. The term "channel" is used here in a general sense, and refers to any medium through which signals are transmitted. For example, a channel may be a radio environment, a copper wire, an optical fiber, or a magnetic storage medium. In each case, the signal received at the receiver differs from the signal transmitted by the transmitter due to the effects of transmission through the channel. The received signal often includes noise and interference from other signals which diminish the quality of the signal and increase the probability of transmission errors.

In wireless communications systems in particular, a phenomenon known as Rayleigh fading may cause highly localized signal losses of 40dB or more due primarily to signal path differences. In order to overcome Rayleigh fading, it is known to employ a plurality of antennas at the receiver in a technique known as spatial diversity. When the receiver antennas are physically separated by a sufficient distance, the signals received by the antennas exhibit uncorrelated Rayleigh fading. The signals

received by the antennas are referred to as "diversity signals," and the antennas are referred to as "diversity antennas." The diversity signals are combined at the receiver to produce a more robust, intelligible signal.

Closely spaced antenna elements may also be used, as in a phased array, to provide array gain, even though diversity gain may be thereby reduced or eliminated. It may be preferable to apply beamforming to phased array signals prior to demodulation.

At the receiver, signal preprocessing operations such as filtering, amplification, and possibly mixing are performed on the signal prior to demodulation. The signal preprocessing operations may also include sampling and quantizing the received signal to obtain a sequence of received data samples. Following such signal preprocessing, the received signal is demodulated and converted to analog for output.

In most digital communication systems, synchronization (or "sync") signals sent by the transmitter assist the receiver in demodulating the received digital signals. The receiver compares the received signals with copies of the known sync signals to determine the bit or symbol timing, to determine frame timing, and possibly to estimate the channel response. The symbol timing indicates the best place to sample the received signal and the frame timing indicates where the start of a new frame occurs. If oversampling is performed, timing indicates which sampling phase to use when decimating the oversampled data.

With conventional synchronization methods, timing is determined by finding a sampling phase which maximizes the signal strength of the desired signal. Typically this is done by correlating the received signal to the sync signal and using magnitude squared correlation values as indications of signal strength.

Unfortunately, the received signal includes an impairment signal that prevents perfect recovery of the transmitted digital symbols. If the impairment is Additive White Gaussian Noise (AWGN), then the conventional strategy of maximizing signal strength described above also maximizes signal-to-noise ratio (SNR) at the input of the demodulator. If the impairment consists of other signals, such as co-channel interference or adjacent channel interference, then the input signal to impairment plus noise ratio (SINR) can be maximized according to the method discussed in U.S. Patent No. 5,406,593 to Chennakeshu et al.

When multiple receive antennas are employed for spatial diversity, the conventional approach is to synchronize each diversity signal separately, as discussed in U.S. Patent No. 5,406,593. This optimizes the SNR or SINR on each diversity channel. This approach makes sense with conventional diversity combining in which no interference cancellation is performed, as the demodulator output SINR is, at best, the sum of the SINRs of the different diversity channels. However, when interference cancellation is performed at the receiver, maximizing the SINR on each antenna is not necessarily the best strategy. Rather, it may be advantageous to coordinate the interfering signals on different antennas in time, so that the interference components of the various signals will cancel one another when the diversity signals are combined. This is something separate channel synchronization cannot guarantee. Thus, there is a need for a method and apparatus capable of jointly synchronizing multiple receive channels to maximize the performance of an interference canceling detector.

SUMMARY OF THE INVENTION

It is, accordingly, a primary object of the present invention to provide an apparatus for joint synchronization of multiple receive channels.

In accordance with the present invention, an apparatus for joint synchronization of multiple receive channels is provided. The apparatus includes means for receiving signals, means for preprocessing received signals, means for joint synchronization of the preprocessed signals, and means for canceling interference in the synchronized signals, wherein the data contents of the received signals are determined after cancellation of the interference.

A method of jointly synchronizing multiple receive signals is further provided. In accordance with the present invention, a sampling phase offset is selected for each diversity signal such that the SINR of the combined receive channels is maximized.

These and other objects of the invention, together with features and advantages thereof, will become apparent from the following detailed description when read with the accompanying drawings in which like reference numerals refer to like elements.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of a typical digital communication system.

Figure 2 is a block diagram of an apparatus for a separate channel synchronization in accordance with the prior art.

Figure 3 is a block diagram of a receiver architecture in accordance with an embodiment of the present invention.

Figure 4 is a block diagram of a joint sync unit in accordance with an embodiment of the present invention.

Figure 5 is a flowchart showing the process of joint synchronization implemented by the joint sync unit of the embodiment of Figure 4.

Figure 6 is a block diagram of a metric computer in accordance with the embodiment of Figure 4.

Figure 7 is a block diagram of another embodiment of a metric computer in accordance with the embodiment of Figure 4.

Figure 8 is a block diagram of a joint sync unit in accordance with another embodiment of the present invention.

Figure 9 is a block diagram of the select unit in accordance with the embodiment of Figure 8.

Figure 10 is a flowchart showing the process of joint synchronization implemented by the joint sync unit of the embodiment of Figure 8.

Figure 11 is a block diagram of a metric computer in accordance with the embodiment of Figure 8.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Figure 1 illustrates a block diagram of a typical digital communication system 10 employing diversity antennas 16a,b wherein digital information symbols s(n) are transmitted as a digital communications signal by a transmitter 12 and a transmit antenna 14. The transmitted signal passes through a transmission medium and is received by receive antennas 16a,b. The receive antennas 16a,b provide the received diversity signals to a receiver 18 which detects the transmitted information symbols. Each diversity signal includes an impairment signal which consists of thermal noise and possibly interference signals. The presence of an impairment signal makes it difficult for the receiver to perfectly detect the information symbols.

Figure 2 illustrates a block diagram of a typical receiver architecture 20 with separate channel synchronization in accordance with prior art. The received signals are processed by signal preprocessors 22a,b, which typically filter, amplify, and mix the signals to baseband signals. Each baseband signal is processed by separate synchronizing means, such as sync units 24a,b, which apply conventional synchronization techniques to determine frame and sample timing. Each individually synchronized diversity signal is then provided to a signal processor 26, which detects the information symbols by analyzing the individually synchronized diversity signals. This is typically done by diversity combining the synchronized signals using well known techniques, such as maximal ratio combining, equal gain combining or selective combining.

In order to improve the accuracy of detection, the signal processor 26 may perform interference cancellation or some other form of demodulation. Interference

cancellation techniques have been proposed for digital communication systems. See, for example, J.H. Winters, Optimum Combining in Digital Mobile Radio with Co-channel Interference, IEEE J. Sel. Areas Commun., vol. 2, pp. 528-539, July 1984 as well as G.E. Bottomley and K. Jamal, Adaptive Arrays and MLSE Equalization, Proc. IEEE Veh. Technol. Conf., Chicago, July 25-28, 1995. The basic principle employed for interference cancellation is to combine signals from the different antennas so that the impairment signals are suppressed or canceled. Thus, the goal is to have the desired signal components from each antenna add constructively, while the interference components add destructively.

However, when interference cancellation is performed in the detector, it is no longer desirable for the sync operation, and in particular the selection of timing, to be designed solely to maximize the signal energy of the desired receive signal. For improved system performance, it is also desirable to reduce the amount of interference present in the received signal after combining the diversity signals. Conceptually, this is achieved by aligning or coordinating the interference components as well as the desired signal components of the diversity signals so that the interference components cancel one another out when combined.

According to the present invention, coordination of the diversity signals is achieved by jointly synchronizing the plurality of diversity signals received at separate antennas. Figure 3 is a block diagram of a receiver architecture in accordance with the present invention. For ease of reference, the present invention will be described with respect to a receiver having two diversity antennas. However, those skilled in the art will recognize that the present invention may be employed in a receiver having more than two diversity antennas, as well as other types of antennas.

In order to facilitate understanding of the present invention, the theory of joint synchronization will be described briefly. The transmitted digital communications signal is received by antennas 21a,b as diversity signals Y_a and Y_b. Antennas 21a,b provide the diversity signals Y_a and Y_b to signal preprocessors 22a and 22b, respectively. The signal preprocessors 22a,b convert the received diversity signals Y_a and Y_b into discrete sample streams, denoted $x_a(k)$ and $x_b(k)$. The discrete sample streams $x_a(k)$ and $x_b(k)$ are then provided to joint sync unit 28, which jointly synchronizes the diversity signals by determining sample timing for each diversity signal. The resulting signals are provided to demodulator 30. In a preferred embodiment, demodulator 30 includes an interference canceling processor.

By taking each of the received signals into account in the synchronization process, the performance of the subsequent interference cancellation process may be optimized in the manner described below. Let $\underline{x}(k)$ denote the vector of received signal samples from signal preprocessors 22a,b, which sample the signal N times per information symbol period. Thus, in a receiver having two receive antennas,

$$\underline{x}(k) = \begin{bmatrix} x_a(k) \\ x_b(k) \end{bmatrix}$$

where each element in the vector corresponds to the signal received by a different receive antenna. The joint sync unit 28 produces a vector of received signal samples denoted $\underline{r}(n)$ sampled only M times per information symbol period, where M is typically 1 or 2. Each element $r_i(n)$ of $\underline{r}(n)$ is given as:

$$[1] \quad r_i(n) = x_i\left(n\frac{N}{M} + p_i\right)$$

where n is the sample index and p_i is an integer value denoting the particular sampling phase selected by the joint sync unit 28 for signal $x_i(k)$. The process of generating $r_i(n)$ from $x_i(k)$ is known as decimation, and is performed by devices known as decimators, which accept $x_i(k)$ and a sampling phase p_i as input.

The collection of sampling phases may be organized as sampling phase vector $\underline{p}$. The joint sync unit 28 selects a set of sampling phases p_i that results in a maximized value of the SINR of the combined signal output by the demodulator 30. The joint sync unit selects one sampling phase per antenna, so that only M out of N samples are kept for processing per symbol period. The receiver is sometimes referred to as being symbol-spaced (M=1) or fractionally spaced (M>1), depending on the choice of M.

By selecting an appropriate sampling phase vector, the output SINR is maximized in the following manner, in which M=1 (i.e. only one sample per period is selected for processing). Taking the array processing method presented in Winters, supra, and omitting the discrete sample index n for simplicity, the vector of received samples $\underline{r}$, after synchronization and sampling, can be represented as:

[2] $\underline{r} = \underline{c}s + \underline{z}$

where $\underline{c}$ is a vector of channel taps, one per antenna, s is the transmitted data symbol to be detected, and $\underline{z}$ is a vector of impairment values, one per antenna. The impairment can include both thermal noise and interference from other communication signals.

To reject both noise and interference, the demodulator 30 combines the samples $\underline{r}$ into a detection statistic y_d which is used to identify the transmitted information symbol s. Of all possible information

symbols, the transmitted information signal is determined to be the one closest to the detection statistic. In the preferred embodiment, the detection statistic y_d is calculated as a weighted average of all received signals. It can be represented by the following equation:

[3] $y_d = \underline{w}^H \underline{r}$

where the superscript H denotes the conjugate transpose of weighting vector $\underline{w}$. According to Winters, supra, an optimal choice for the weights is given by:

[4] $\underline{w} = R^{-1}_{zz}\underline{c}$

where $R_{zz} = E\{\underline{z}\,\underline{z}^H\}$ is the expected value of the correlation matrix associated with the impairment across the receive antennas 21a,b. For a system having D receive antennas, R_{zz} comprises a matrix having dimensions DxD. $E\{x\}$ denotes expected value of x. The zz subscript indicates that R is obtained by correlating the impairment vector $\underline{z}$ with itself ($\underline{z}$). In practice, the channel taps $\underline{c}$ and the impairment correlation matrix R^{-1}_{zz} can be estimated from the received signal using conventional methods. An example of such estimation is given in U.S. Application Ser. No. 08/284,775, which is incorporated herein by reference.

Theoretically, the output SINR using this technique is given in Winters, supra, by the following equation:

[5] $SINR = \underline{c}^H R^{-1}_{zz}\underline{c}$

However, the values for the channel taps and the impairment correlation matrix will depend on the sync or timing used, which is denoted by the sampling phase vector $\underline{p}$. Thus, in general, the output SINR is given by:

[6] $SINR(\underline{p}) = \underline{c}^{H}(\underline{p})R^{-1}_{zz}(\underline{p})\underline{c}(\underline{p})$

From equation 6 it is observed that the output SINR depends on the entire sampling phase vector and that maximizing SINR cannot be achieved by selecting the sampling phase of each antenna signal independently.

To optimize output SINR, coordinated synchronization of the diversity signals (i.e. "joint sync") is performed. In other words, by determining the sampling phases p_i collectively instead of individually, output SINR is maximized. In the present invention, joint synchronization is accomplished by considering various test sampling phase vectors $\underline{p}'$. The output SINR is estimated for each test sampling phase vector $\underline{p}'$. The test sampling phase vector $\underline{p}'$ that maximizes the output SINR is selected and used by the receiver to decimate the received signals. To reduce complexity, separate channel synchronization may be performed first, so that only a limited number of candidate sampling phase vectors about the separate sync result need be tested.

Figure 4 illustrates a joint sync unit 28 in accordance with an embodiment of the present invention. Joint sync unit 28 includes a decimator 70, a control unit 72, a metric computer 74 and a double pole-single throw switch 76. Prior to processing, switch 76 is open to prevent spurious values of $r_i(n)$ from being passed to the demodulator 30.

Received signals $x_a(k)$ and $x_b(k)$ are provided to decimator 70. Received signals $x_a(k)$ and $x_b(k)$ may be buffered by one or more input buffers (not shown). The sampling phase vector $\underline{p}$ is provided to decimator 70 by control unit 72. Decimator 70 produces decimated signals $r_a(n)$ and $r_b(n)$ as output. Metric computer 74 receives decimated signals $r_a(n)$ and $r_b(n)$ and uses them to calculate a metric which predicts the performance of the

subsequent process of interference cancellation. In the preferred embodiment, the metric is an estimate of the signal to impairment plus noise ratio (SINR) at the output of the receiver.

The control unit 72 provides various test sampling phase vectors $\underline{p}'$ to the decimator 70, and selects the sampling phase vector that results in the highest output SINR estimate.

The initial test sampling phase vector $\underline{p}'$ evaluated may be a previously selected sampling phase vector selected or it may be obtained through customary synchronization processing. In one embodiment of the present invention, a predetermined range of test sampling phase vectors near the initial sampling phase vector are evaluated, and the test sampling phase vector that produces the highest output SINR is selected and used to synchronize the diversity signals. However, it will be understood that other algorithms for selecting a test sampling phase vector may be employed without departing from the spirit or scope of the present invention.

Once the control unit 72 has identified the optimal sampling phase vector $\underline{p}_{opt}$, the control unit 72 provides $\underline{p}_{opt}$ to the decimator 70 and closes switch 76. Decimated signals $r_a(n)$ and $r_b(n)$ are thus provided to demodulator 30.

Figure 5 illustrates a possible logic flow for control unit 72. First, switch 76 is opened and an initial value for $\underline{p}_{opt}$ is selected. As described above, the initial value for $\underline{p}_{opt}$ may be a previously selected value, or it may be obtained through customary synchronization techniques.

Next, $\underline{p}_{opt}$ is output to decimator 70, which uses $\underline{p}_{opt}$ to decimate received signals $x_a(k)$ and $x_b(k)$.

Then, a SINR estimate generated as a result of the use of $\underline{p}_{opt}$ as the sampling phase vector is input from metric computer 74.

Next, a test sampling phase vector $\underline{p}'$ is generated by control unit 72. The generation of test sampling phases may be accomplished by any one of several algorithms. For example, the control unit may select one of a number of sampling phase vectors near the initial sampling phase vector. Or, the control unit may select and evaluate each possible sampling phase vector in turn.

Next, the selected test sampling phase vector $\underline{p}'$ is provided to decimator 70, which uses $\underline{p}'$ to decimate received signals $x_a(k)$ and $x_b(k)$.

Then, a SINR estimate generated as a result of the use of $\underline{p}'$ as the sampling phase vector is input from metric computer 74.

Next the SINR estimate based on $\underline{p}'$ is compared with the SINR estimate based on $\underline{p}_{opt}$. If the SINR estimate based on $\underline{p}'$ is greater than the SINR estimate based on $\underline{p}_{opt}$, then $\underline{p}_{opt}$ is set equal to $\underline{p}'$, and the maximum SINR estimate is updated.

The control unit then determines whether to evaluate another test sampling phase vector. This decision will depend on whether all values of $\underline{p}'$ of interest have already been evaluated and may depend on whether an adequate SINR has been obtained. The control unit may also be forced by time or processing limitations to stop evaluating test values of $\underline{p}$ before all vectors of interest have been evaluated.

If the control unit determines that evaluation should continue, a new value of $\underline{p}'$ is selected, and processed as described above.

If the control unit determines that processing is complete and no further test sampling phase vector should be evaluated, then $\underline{p}_{opt}$ is output to the decimator 70 and switch 76 is closed.

Figure 6 illustrates a block diagram of a metric computer 74 in accordance with the embodiment of Figure 4. Decimated samples $r_i(n)$ of the received signals are

provided to channel tap estimators 32a,b, which estimate the signals' channel tap delays and coefficients c_{est} using conventional techniques. These estimates are passed on to combiners 34a,b, which use known or detected information symbols and the channel tap coefficients to form estimates of the received signals, denoted in vector form as $r_{est}(k)$. Known information symbols may be used when the receiver is processing a set of predetermined information symbols, such as is the case, for example, during synchronization processing.

Delay units 38a,b impart a delay to the received signals equal to the delay imparted to the estimated received signals by the channel estimators 32a,b. The received signal estimates are subtracted from the received signals by adders 36a,b.

The outputs $z_{i,est}(n)$ of the adders 36a,b are estimates of the impairment components of the received signals. The impairment component estimates are denoted collectively as vector $z_{est}(k)$. The impairment estimates are then passed on to inverse correlation estimator 40, which generates an estimate of the inverse correlation matrix R^{-1}_{zz}. The inverse correlation matrix R^{-1}_{zz} can be estimated directly using matrix inversion lemma approaches well known in the art, or it can be obtained by estimating and then inverting the correlation matrix. Other approaches are possible also, including estimation of the square root of the matrix or an LDU factorization.

The channel tap coefficients and the inverse correlation matrix estimate are passed on to arithmetic logic processor 42, which uses the provided values to calculate an estimate of the output SINR. The SINR estimate is then provided to the control unit 72, as described above. As new information symbols are continuously being received and processed by the receiver, the SINR estimates tend to change with time. Because the SINR estimates may be noisy and the optimal

Fig. 4

sampling phase vector may be changing slowly, it is desirable to smooth the SINR estimates in time, for example by using a low pass filter [not shown].

Other metrics related to output SINR or demodulator performance may be employed, such as replacing R_{zz} with R_{rr}, the data correlation matrix, which is simpler to estimate. This approach is illustrated in Figure 7, which shows a metric computer 74' which includes a data correlation estimator 41, a pair of channel estimators 32a,b, and an arithmetic logic processor 42. The data correlation estimator 41 accepts as input the decimated signals $r_a(n)$ and $r_b(n)$ and generates an estimate of the data correlation matrix R_{rr} therefrom. Channel estimators 32a,b generate channel tap estimates c_a and c_b for the channels based on the decimated signals $r_a(n)$ and $r_b(n)$. The channel tap estimates c_a and c_b and the data correlation matrix R_{rr} are provided to the arithmetic logic processor 42, which calculates a metric to be optimized. The metric is calculated according to the following equation:

[7] $$\text{metric} = \underline{c}^H R^{-1}_{rr} \underline{c}$$

Figure 8 illustrates another embodiment of the joint sync unit of the present invention. As illustrated in Figure 8, joint sync unit 105 includes a select unit 100 and a metric computer 103. Select unit 100 receives signals $x_a(k)$ and $x_b(k)$ as input, and produces decimated signals $r_a(n)$ and $r_b(n)$ as output. Select unit 100 also generates test sampling phase vectors $\underline{p}'$ and outputs the test vectors to metric computer 103. Metric computer 103 accepts signals $x_a(k)$ and $x_b(k)$ as input along with the test sampling phase vector $\underline{p}'$ and generates an estimate of output SINR, which is provided to select unit 100.

As illustrated on Figure 9, select unit 100 includes control unit 101 and decimator 102. Control unit 101

accepts a SINR estimate generated by metric computer 103 as input. Control unit 101 outputs an optimal sampling phase vector $\underline{p}_{opt}$ to decimator 102, which uses $\underline{p}_{opt}$ to decimate input signals $x_a(k)$ and $x_b(k)$. Control unit 101 also outputs a test sampling phase vector $\underline{p}'$ to metric computer 103, which calculates a SINR estimate based on the provided test sampling phase vector $\underline{p}'$.

By using separate decimators in the select unit and the metric computer, the joint sync unit 105 of Figure 8 has the capability of continuously evaluating different sampling phase vectors while the select unit 100 continues to process incoming signals using a previously selected sampling phase. This feature is useful in broadband communication systems, wherein it may be impossible or inconvenient to buffer an incoming sample stream for processing.

Figure 10 illustrates a possible logic flow for control unit 101. First, an initial value for $\underline{p}_{opt}$ is selected and provided to decimator 102. As described above, the initial value for $\underline{p}_{opt}$ may be a previously selected value, or it may be obtained through customary synchronization techniques.

Next, $\underline{p}_{opt}$ is output to metric computer 103, which uses $\underline{p}_{opt}$ to decimate received signals $x_a(k)$ and $x_b(k)$.

Then, a SINR estimate generated as a result of the use of $\underline{p}_{opt}$ as the sampling phase vector is output from metric computer 103 to select unit 100.

Next, a test sampling phase vector $\underline{p}'$ is generated by control unit 101 and provided to metric computer 103, which uses the test sampling phase vector $\underline{p}'$ to decimate received signals $x_a(k)$ and $x_b(k)$.

Then, a SINR estimate generated as a result of the use of $\underline{p}'$ as the sampling phase vector is output from metric computer 103 to select unit 100.

Next the SINR estimate based on $\underline{p}'$ is compared with the SINR estimate based on $\underline{p}_{opt}$. If the SINR estimate

based on $\underline{p}'$ is greater than the SINR estimate based on $\underline{p}_{opt}$, then $\underline{p}_{opt}$ is set equal to $\underline{p}'$ when appropriate, and the maximum SINR estimate is updated.

The control unit then determines whether to evaluate another test sampling phase vector. This decision will depend on whether all values of $\underline{p}'$ of interest have already been evaluated. The control unit may also be forced by time or processing limitations to stop evaluating test values of $\underline{p}$ before all vectors of interest have been evaluated.

If the control unit determines that evaluation should continue, a new value of $\underline{p}'$ is selected, and processed as described above.

If the control unit determines that processing is complete and no further test sampling phase vector should be evaluated, then $\underline{p}_{opt}$ is output to the decimator 102.

Figure 11 illustrates, in block diagram format, metric computer 103 in accordance with the embodiment of Figure 8. Metric computer 103 includes decimators 104a,b, which accept received signals $x_a(k)$ and $x_b(k)$ as input along with test sampling phase values p_a' and p_b', respectively, and generate decimated signals $r_a(n)$ and $r_b(n)$, respectively.

Decimated signals $r_a(n)$ and $r_b(n)$ are provided to channel tap estimators 32a,b, which estimate the signals' channel tap coefficients $\underline{c}_{est}$ using conventional techniques. These estimates are passed on to combiners 34a,b, which use known or detected information symbols and the channel tap coefficients to form estimates of the received signals denoted $\underline{r}_{est}(k)$.

Delay units 38a,b impart a delay to the received signals equal to the delay imparted to the estimated received signals by the channel estimators 32a,b. The received signal estimates are subtracted from the received signals by adders 36a,b.

The outputs $z_{i,est}(k)$ of the adders 36a,b are estimates of the impairment components of the received signals. The impairment estimates are then passed on to inverse correlation estimator 40, which generates an estimate of the inverse correlation matrix R^{-1}_{zz}.

The channel tap coefficients and the inverse correlation matrix estimate are passed on to arithmetic logic processor 42, which uses the provided values to calculate an estimate of the output SINR. The SINR estimate is then provided to the select unit 100, as described above.

The present invention is readily extendible to an interference cancellation scheme given by Bottomley wherein the interference cancellation processor also equalizes the received signal. In that case, the received signal includes echoes which are delayed versions or images of the received signal. In the case of two received versions, a main version and an echo, the received signal after sync can be modeled as:

[8] $\underline{r}'(n) = \underline{c}_0 s(n) + \underline{c}_1 s(n-1) + \underline{z}(n)$

assuming one sample per symbol (M=1).

Thus, from the foregoing equation it is observed that the channel taps comprise vectors, $\underline{c}_0$ and $\underline{c}_1$, one vector per image or echo. Channel estimators 32 would estimate these channel taps and signal generator units 34 would use these estimates to remove the images, leaving estimates of the vectors of impairment values z(n). The metric computer 42 would estimate SINR as follows:

[9] $SINR(p) = \underline{c}_0^H(p) R^{-1}_{zz}(p) \underline{c}_0(p) + \underline{c}_1^H(p) R^{-1}_{zz}(p) \underline{c}_1(p)$

Other metrics are possible.

The present invention is also readily extended to fractionally-spaced demodulation, in which more than one sample per symbol period is required. When M>1, SINR terms for each interleaved, symbol-spaced data stream can be added together.

While the invention has been described with regard to a receiver having two receive antennas, it will be appreciated by those skilled in the art that the invention may be applied to a receiver having any number of receive antennas, which antennas may not necessarily be widely spaced. Moreover, although the invention has been described with regards to multiple receive antennas, it is applicable to any multiple channel receiver, wherein the multiple channels could correspond to beams, different polarizations, or other channel forms. Also, the desired signal may be a set of desired signals that are jointly demodulated.

The present invention may also be applied to a variety of demodulation techniques, including linear and decision feedback equalization, as well as symbol-by-symbol MAP detection. The desired signal may be modulated in a variety of ways, including QPSK, $\pi/4$-DQPSK, GMSK and coded modulation. The demodulation process typically produces soft bit or symbol values which are further processed for channel decoding, such as block, convolutional or turbo decoding. Finally, the present invention is also applicable when "sync" symbols are absent or not known. Different hypotheses of the transmitted signals can be considered. For each hypothesis, the optimal sampling phase and SINR can be determined. The hypothesis and sampling phase that maximize SINR determine the sampling phase to use.

While the present invention has been described with respect to its preferred embodiment, those skilled in the art will recognize that the present invention is not limited to the specific embodiment described and

illustrated herein. Different embodiments and adaptations besides those shown herein and described as well as many variations, modifications and equivalent arrangements will now be apparent or will be reasonably suggested by the foregoing specification and drawings, without departing from the substance or scope of the invention. While the present invention has been described herein in detail in relation to its preferred embodiment, it is also understood that this disclosure is only illustrative and exemplary of the present invention and is made merely for purpose of providing a full and enabling disclosure of the invention. Accordingly, it is intended that the invention be limited only by the spirit and scope of the claims appended hereto.

What is claimed is:

1. An apparatus for synchronizing a signal received over a first receive channel in a radio receiver, the radio receiver having multiple receive channels and a demodulator, the apparatus comprising:

first means for receiving a first signal corresponding to the first receive channel;

second means for receiving a second signal corresponding to a second receive channel; and

synchronizing means, responsive to said first means and said second means, for synchronizing the first signal operative as a function of the first signal and the second signal.

2. The apparatus of claim 1, wherein said synchronizing means includes:

a control unit for generating a sampling phase for use in synchronizing the first signal;

a decimator, connected to said first means and said control unit, for decimating the first signal responsive to the sampling phase generated by said control unit; and

a metric computer responsive to said decimator, for generating a metric predictive of the performance of the demodulator.

3. The apparatus of claim 2, wherein said control unit receives the metric generated by said metric computer and generates the sampling phase in response to the metric.

4. The apparatus of claim 3, wherein said synchronizing means includes a switch controlled by said

control unit, said switch having a first position and a second position, wherein when in the first position, said switch is operative to permit the apparatus to output decimated signals to the demodulator, and when in the second position, said switch is operative to prevent the apparatus from outputting decimated signals to the demodulator.

5. The apparatus of claim 3, wherein the metric generated by said metric computer includes an estimate of the signal to impairment plus noise ratio of the demodulator output.

6. The apparatus of claim 5 wherein said metric computer comprises:

at least two channel estimators for estimating channel tap coefficients corresponding to the first signal and the second signal;

at least two delay units for delaying the first and second signals;

at least two combiners, each connected to one of said channel estimators, for combining known or detected information symbols with channel tap coefficients, to produce desired signal values; and

at least two adders, each connected to one of said combiners and one of said delay units, for subtracting the desired signal values from the delayed signals to produce impairment components of the first and second signals.

7. The apparatus of claim 6, wherein said metric computer further comprises:

an inverse correlation estimator, connected to said adders, for generating an estimated inverse correlation matrix from the impairment components of the first and second signals; and

an arithmetic logic processor, connected to said inverse correlation estimator and said channel estimators, for forming the metric from the inverse correlation matrix and the channel tap coefficients.

8. The apparatus of claim 5 wherein said metric computer comprises:

at least two channel estimators for estimating channel tap coefficients for the first signal and the second signal;

a data correlation estimator for estimating a data correlation matrix for the first and second signals; and

an arithmetic logic processor, connected to said data correlation estimator and said channel estimators, for forming the metric from the data correlation matrix and the channel tap coefficients.

9. The apparatus of claim 1, wherein the demodulator includes an interference canceling processor.

10. An apparatus for synchronizing a signal received over a first receive channel in a radio receiver, the radio receiver having multiple receive channels and a demodulator, the apparatus comprising:

first means for receiving a first signal corresponding to the first receive channel;

second means for receiving a second signal corresponding to a second receive channel;

synchronizing means for synchronizing the first signal operative as a function of the first signal and the second signal, wherein said synchronizing means includes a select unit connected to said first means and said second means and a metric computer for generating a metric predictive of the performance of the demodulator connected to said first means and said second means.

11. The apparatus of claim 10, wherein said select unit includes:

a control unit for generating a test sampling phase and a selected sampling phase for use in synchronizing the first signal; and

a decimator for decimating the first signal responsive to the selected sampling phase generated by said control unit.

12. The apparatus of claim 11 wherein said metric computer comprises:

at least one decimator for decimating the first signal responsive to the test sampling phase generated by said select unit;

at least two channel estimators for estimating channel tap coefficients corresponding to the first signal and the second signal;

at least two delay units for delaying the first and second signals;

at least two combiners, each connected to one of said channel estimators, for combining known or detected information symbols with channel tap coefficients, to produce desired signal values; and

at least two adders, each connected to one of said combiners and one of said delay units, for subtracting the desired signal values from the delayed signals to produce impairment components of the first and second signals.

13. The apparatus of claim 12, wherein said metric computer further comprises:

an inverse correlation estimator, connected to said adders, for generating an estimated inverse correlation matrix from the impairment components of the first and second signals; and

an arithmetic logic processor, connected to said inverse correlation estimator and said channel estimators, for forming the metric from the inverse correlation matrix and the channel tap coefficients.

14. The apparatus of claim 13, wherein the metric generated by the arithmetic logic processor includes an estimate of the signal to impairment plus noise ratio of the demodulator output.

15. The apparatus of claim 10, wherein the demodulator includes an interference canceling processor.

16. A method for joint synchronization of signals received over multiple receive channels in a radio

receiver having a demodulator, the method comprising the steps of:

generating a set of test sampling phase vectors;

decimating the signals responsive to the test sampling phase vectors, thereby producing decimated signals;

for each test sampling phase vector, generating a metric predictive of the performance of the demodulator based on such test sampling phase vector;

selecting the test sampling phase vector that optimizes performance of the demodulator; and

decimating the signals responsive to the selected sampling phase vector.

17. The method of claim 16, further including the step of:

upon selection of a sampling phase vector that optimizes performance of the demodulator, closing a switch to permit the output of decimated signals to the demodulator.

18. The method of claim 16, wherein the demodulator includes an interference canceling processor.

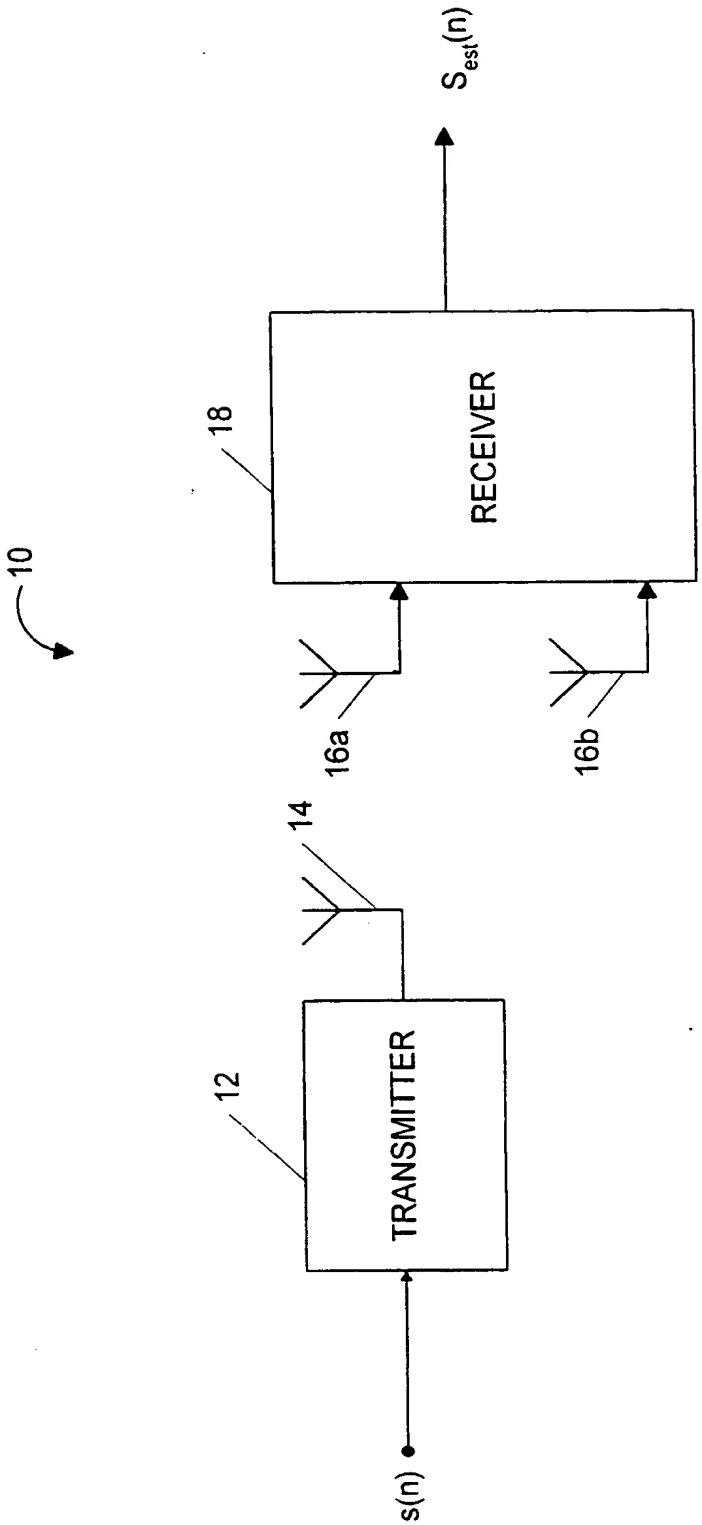


FIGURE 1

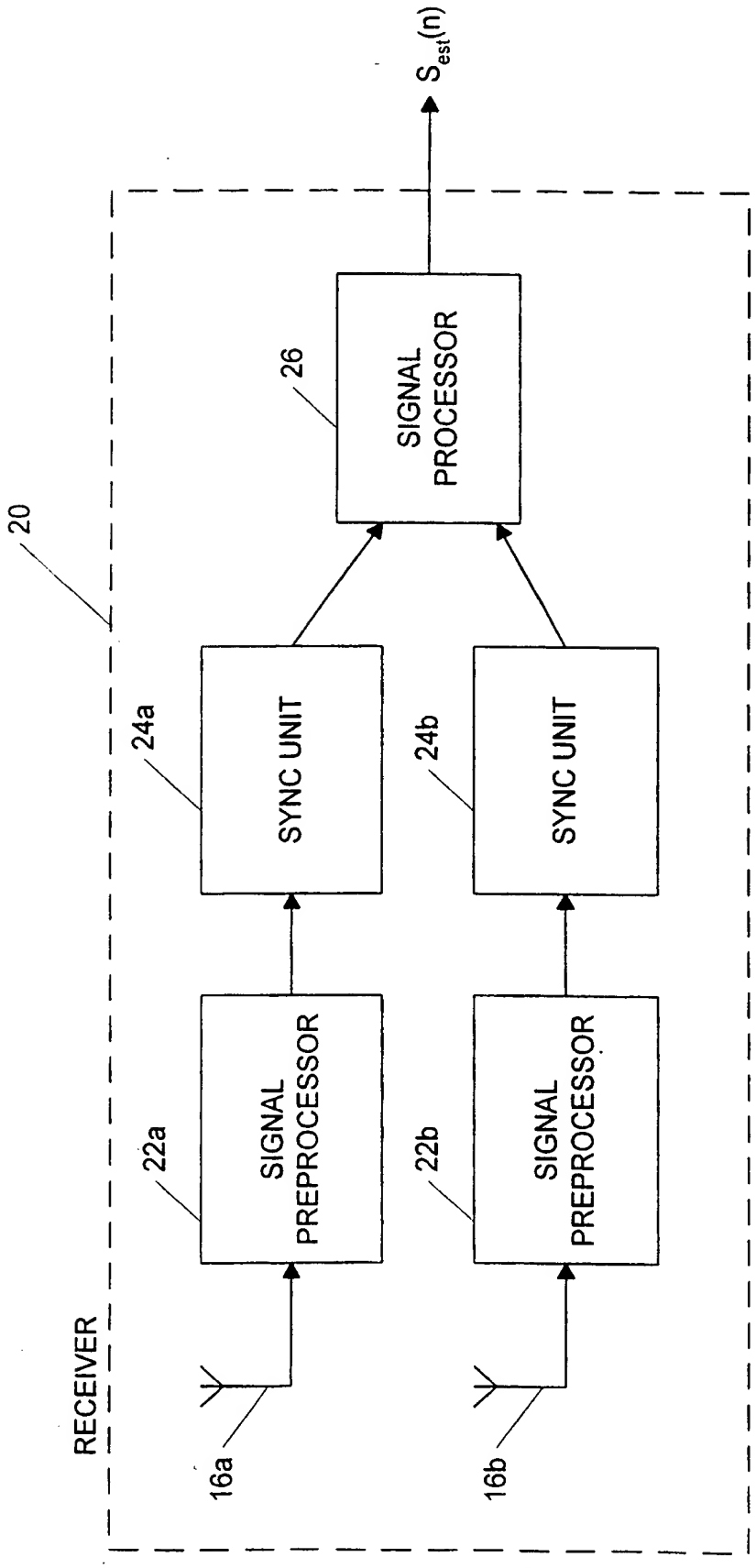


FIGURE 2

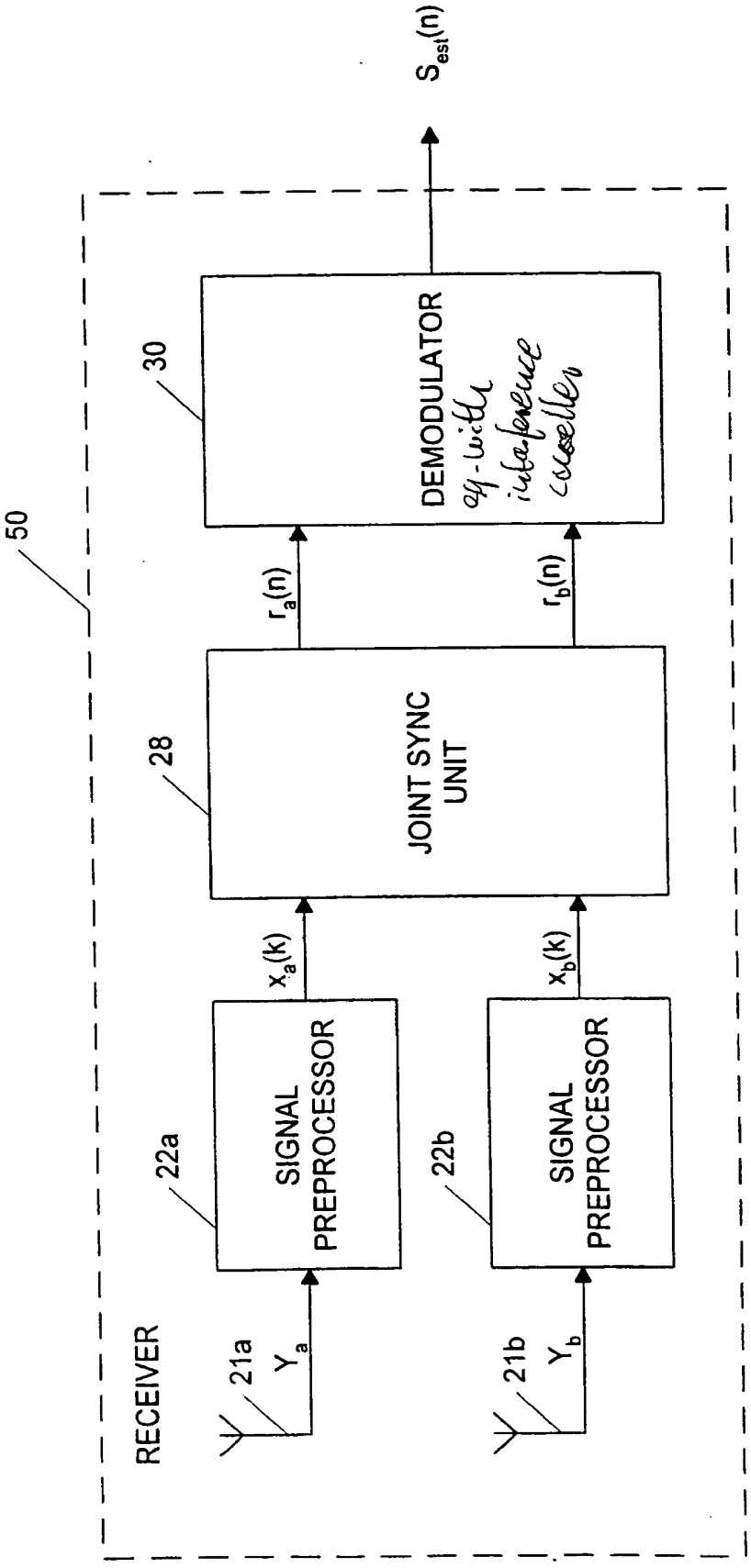


FIGURE 3

invention

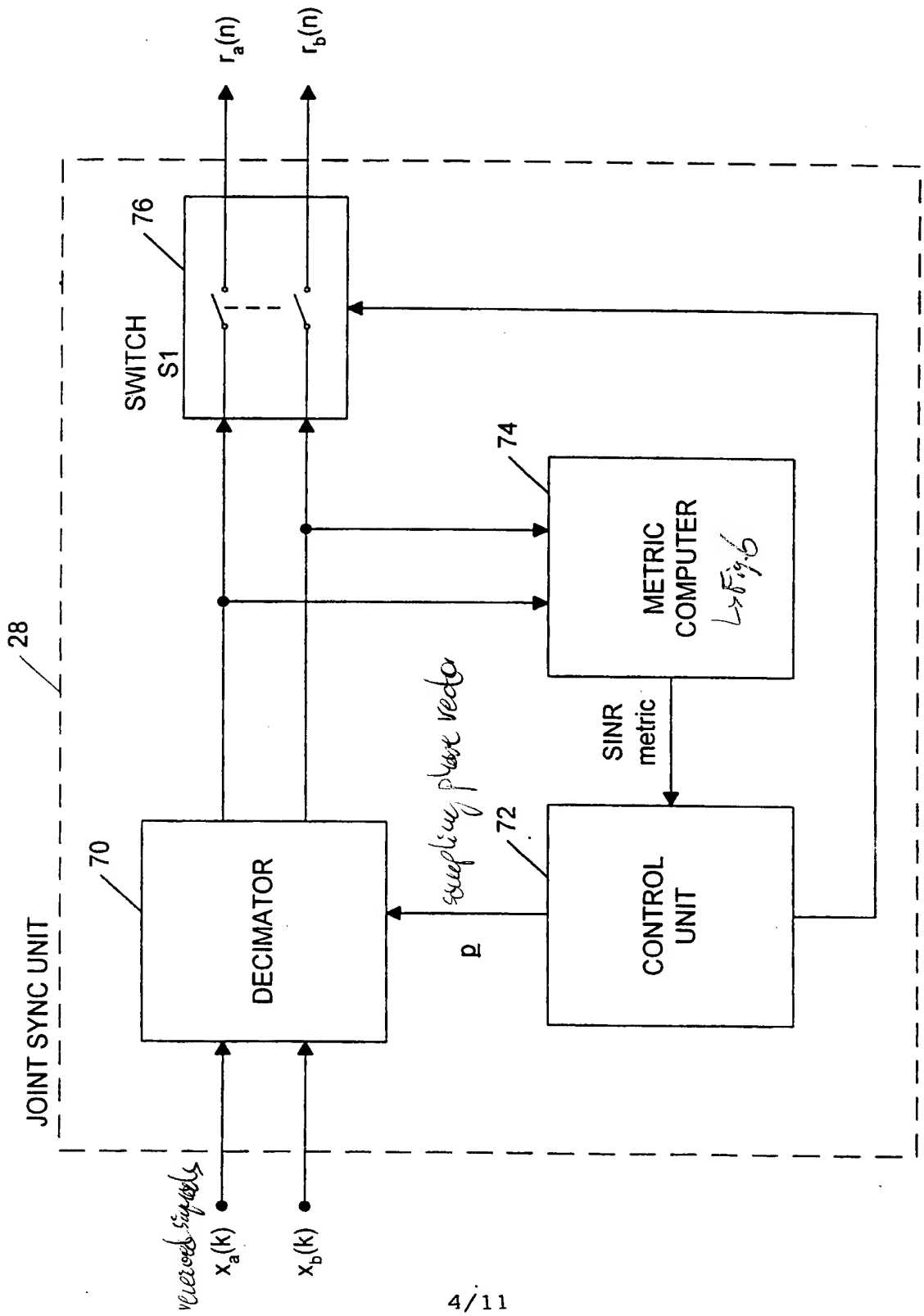


FIGURE 4

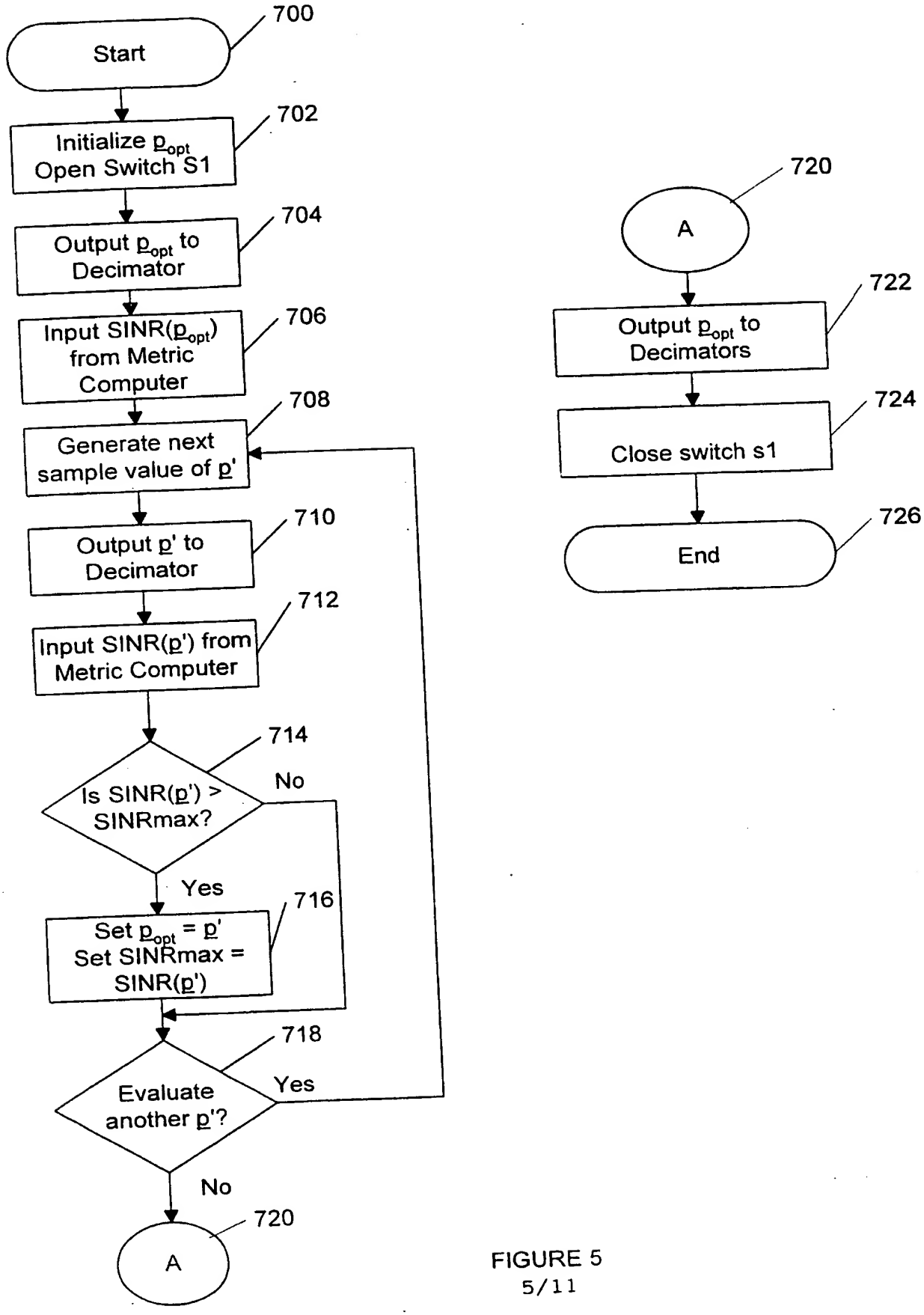


FIGURE 5
5/11

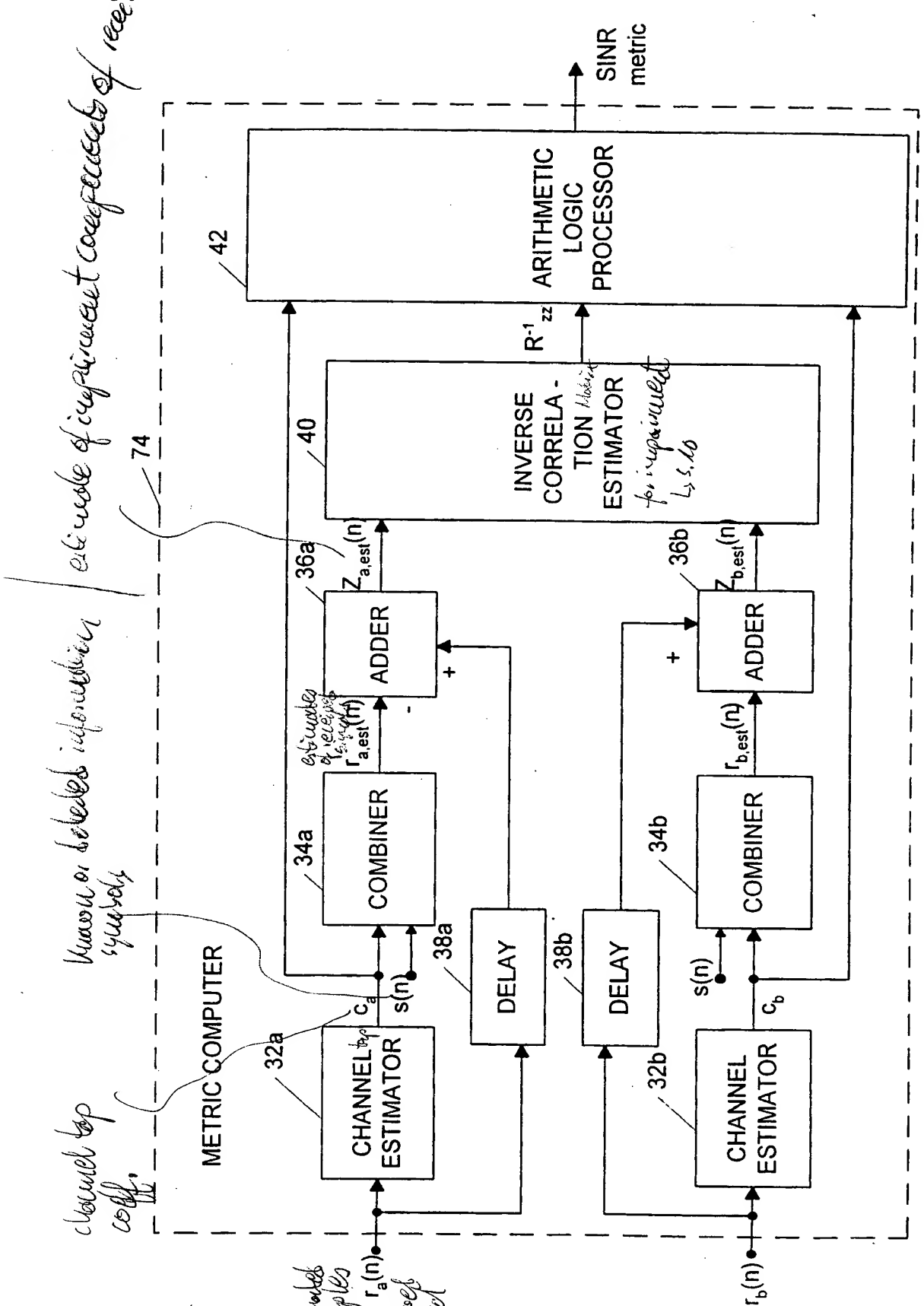

SINR metric
42
ARITHMETIC LOGIC PROCESSOR
R^{-1}_{zz}
40
INVERSE CORRELA-TION ESTIMATOR
74
36a
$Z_{a,est}(n)$
ADDER
$r_{a,est}(n)$
34a
COMBINER
c_a
s(n)
38a
DELAY
32a
CHANNEL ESTIMATOR
$r_a(n)$
36b
$Z_{b,est}(n)$
ADDER
$r_{b,est}(n)$
34b
COMBINER
c_b
s(n)
38b
DELAY
32b
CHANNEL ESTIMATOR
$r_b(n)$
METRIC COMPUTER

FIGURE 6

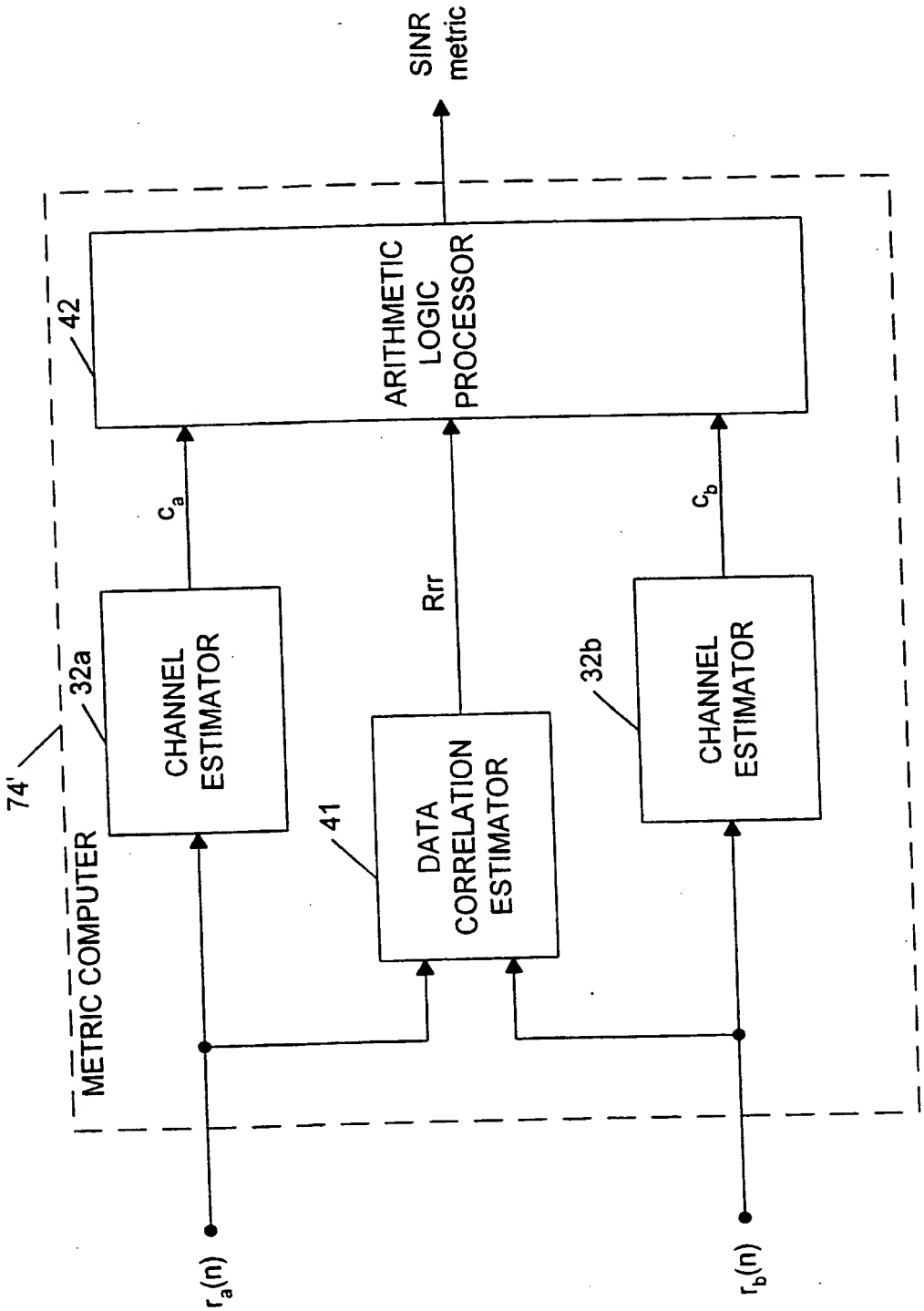


FIGURE 7 alternative to Fig-6

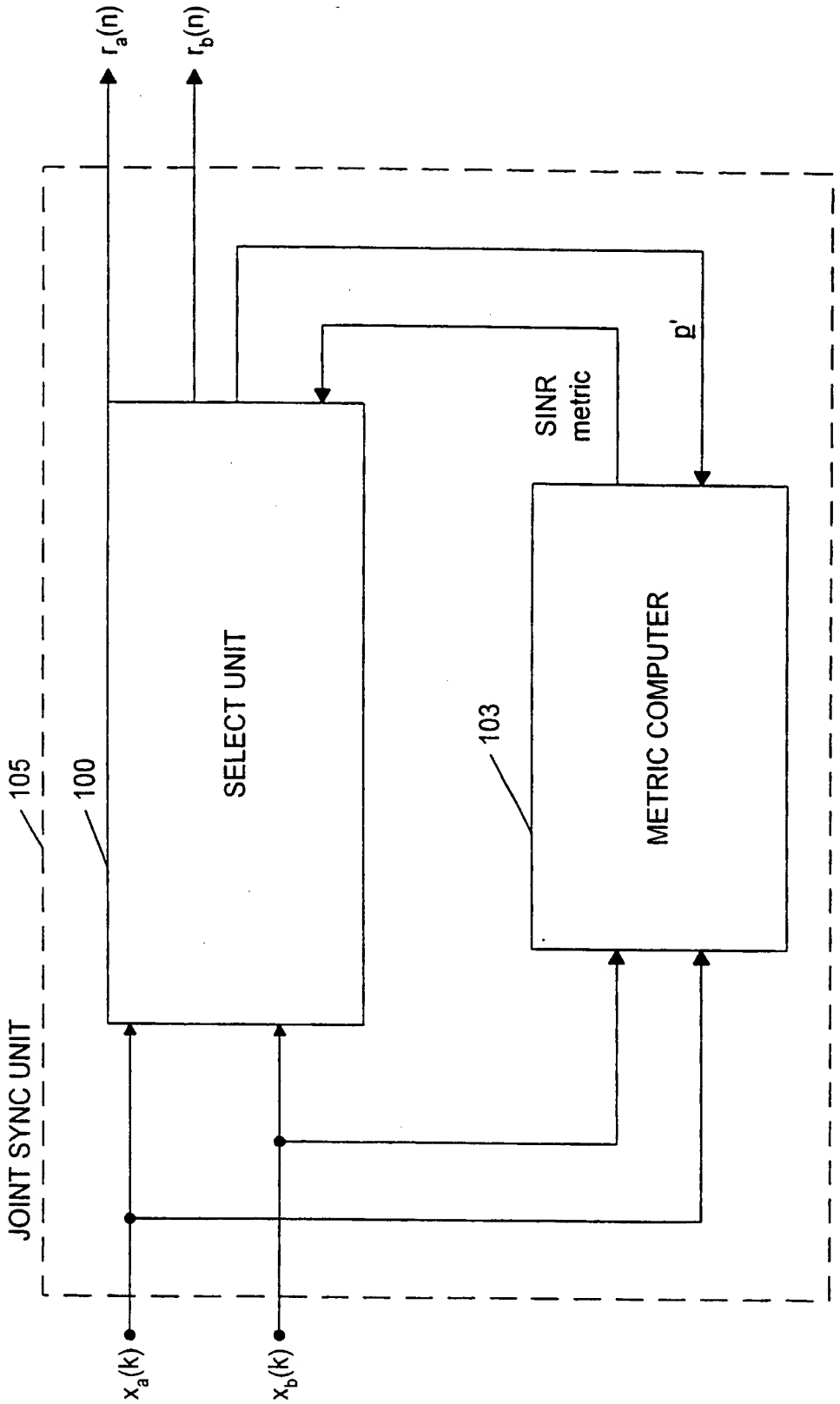


FIGURE 8

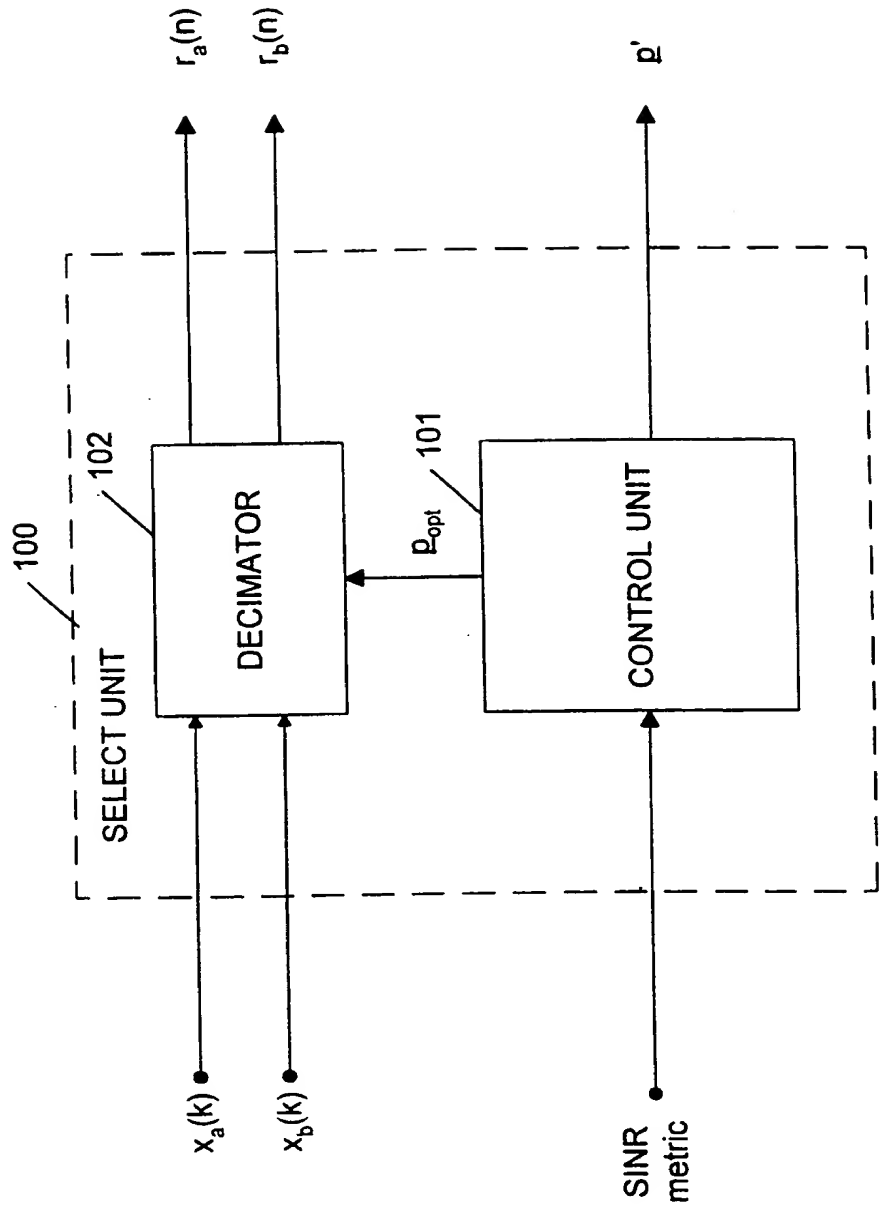

$r_a(n)$
$r_b(n)$
p'
100
SELECT UNIT
102
DECIMATOR
p_{opt}
101
CONTROL UNIT
$x_a(k)$
$x_b(k)$
SINR metric

FIGURE 9

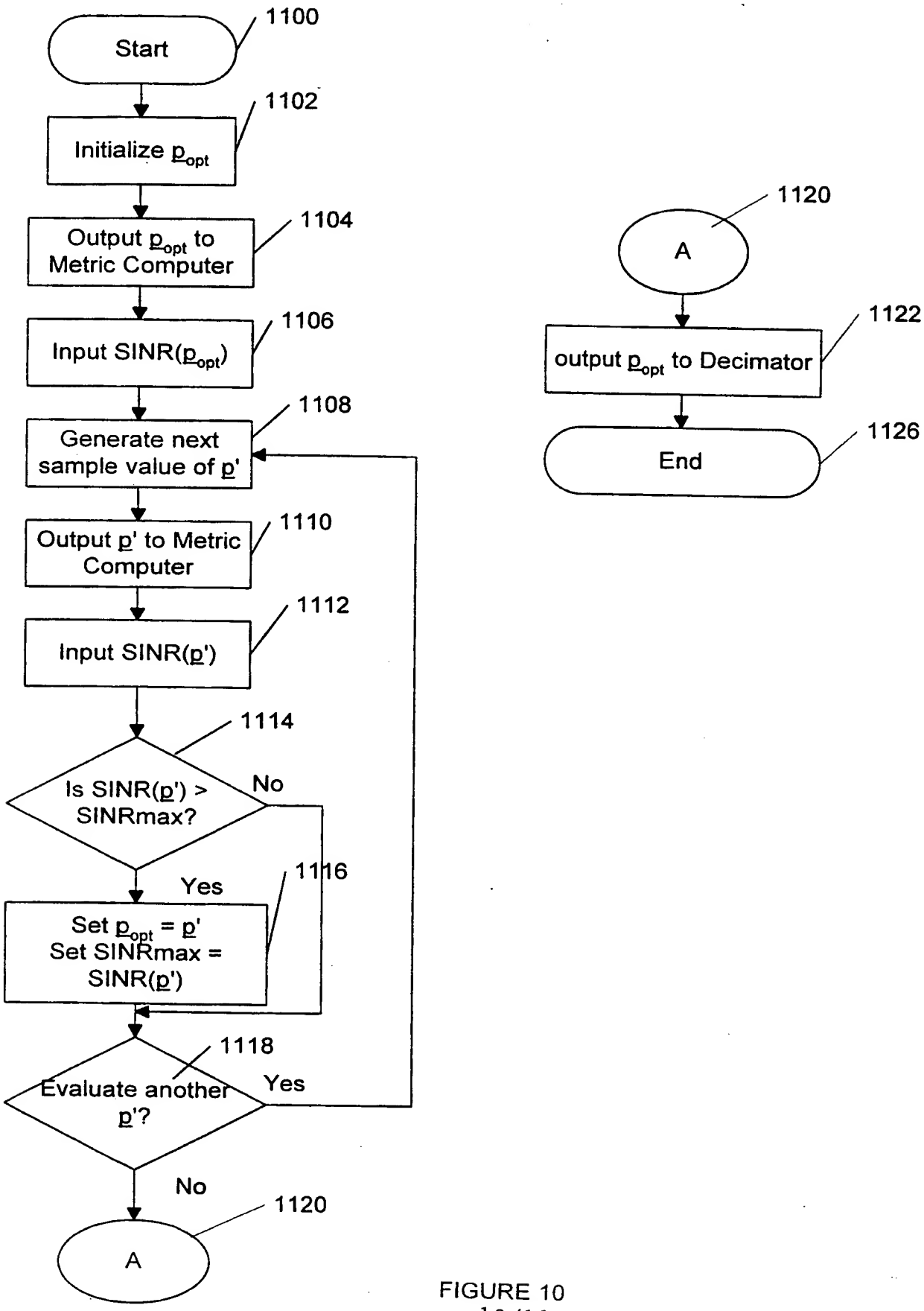


FIGURE 10

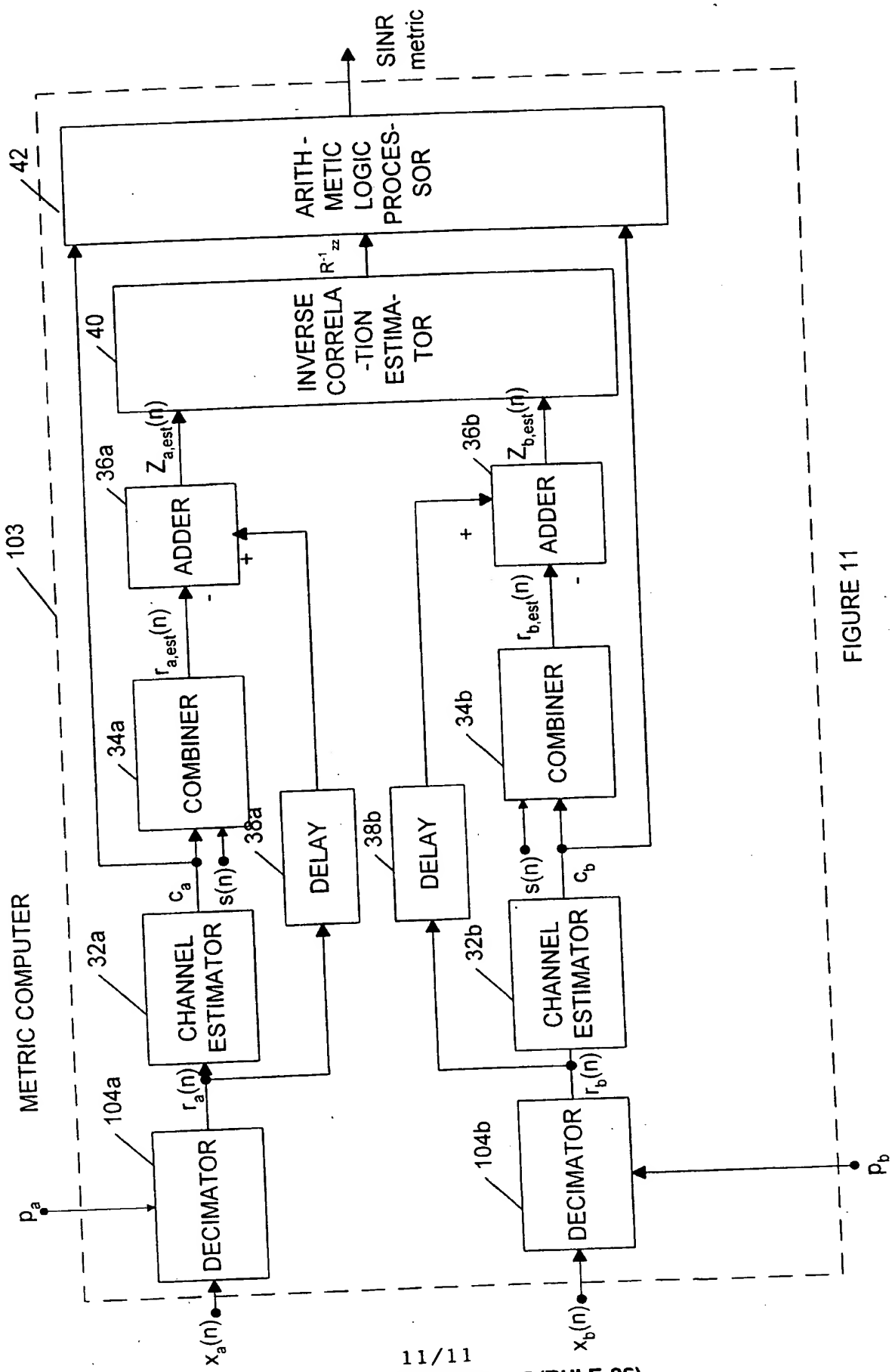

SINR metric
42
ARITH-METIC LOGIC PROCES-SOR
40
INVERSE CORRELA-TION ESTIMA-TOR
R^{-1}_{zz}
103
METRIC COMPUTER
36a
ADDER
$Z_{a,est}(n)$
36b
ADDER
$Z_{b,est}(n)$
34a
COMBINER
$r_{a,est}(n)$
34b
COMBINER
$r_{b,est}(n)$
38a
DELAY
38b
DELAY
32a
CHANNEL ESTIMATOR
32b
CHANNEL ESTIMATOR
c_a
c_b
s(n)
s(n)
104a
DECIMATOR
104b
DECIMATOR
$r_a(n)$
$r_b(n)$
p_a
p_b
$x_a(n)$
$x_b(n)$

FIGURE 11

INTERNATIONAL SEARCH REPORT

Inter..ational Application No
PCT/US 97/22042

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04B7/08

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04B H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 716 513 A (NIPPON ELECTRIC CO) 12 June 1996 see column 6, line 21 - line 55; figures 3,8 see column 11, line 5 - line 45	1,10
X	EP 0 544 315 A (NIPPON ELECTRIC CO) 2 June 1993 see abstract; claims 1-4; figure 1	16
A	WO 96 07247 A (MOTOROLA INC) 7 March 1996 see abstract; claims 1-4; figure 2	1,2,10
A	US 5 406 593 A (CHENNAKESHU SANDEEP ET AL) 11 April 1995 cited in the application see the whole document	1,10

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

2

Date of the actual completion of the international search	Date of mailing of the international search report
17 March 1998	24. 04. 98
Name and mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Authorized officer Kolbe, W

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 97/22042

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0716513 A	12-06-96	JP 2689926 B	10-12-97
		JP 8163103 A	21-06-96
		US 5701333 A	23-12-97
EP 0544315 A	02-06-93	JP 2683665 B	03-12-97
		JP 5152975 A	18-06-93
		CA 2083749 A	28-05-93
		US 5444721 A	22-08-95
WO 9607247 A	07-03-96	US 5621770 A	15-04-97
		BR 9506344 A	05-08-97
		CA 2174242 A	07-03-96
		CN 1134767 A	30-10-96
		DE 19581148 T	19-12-96
		FI 961736 A	22-04-96
		JP 9504936 T	13-05-97
		SE 9601586 A	25-06-96
US 5406593 A	11-04-95	NONE	